FIG. 1

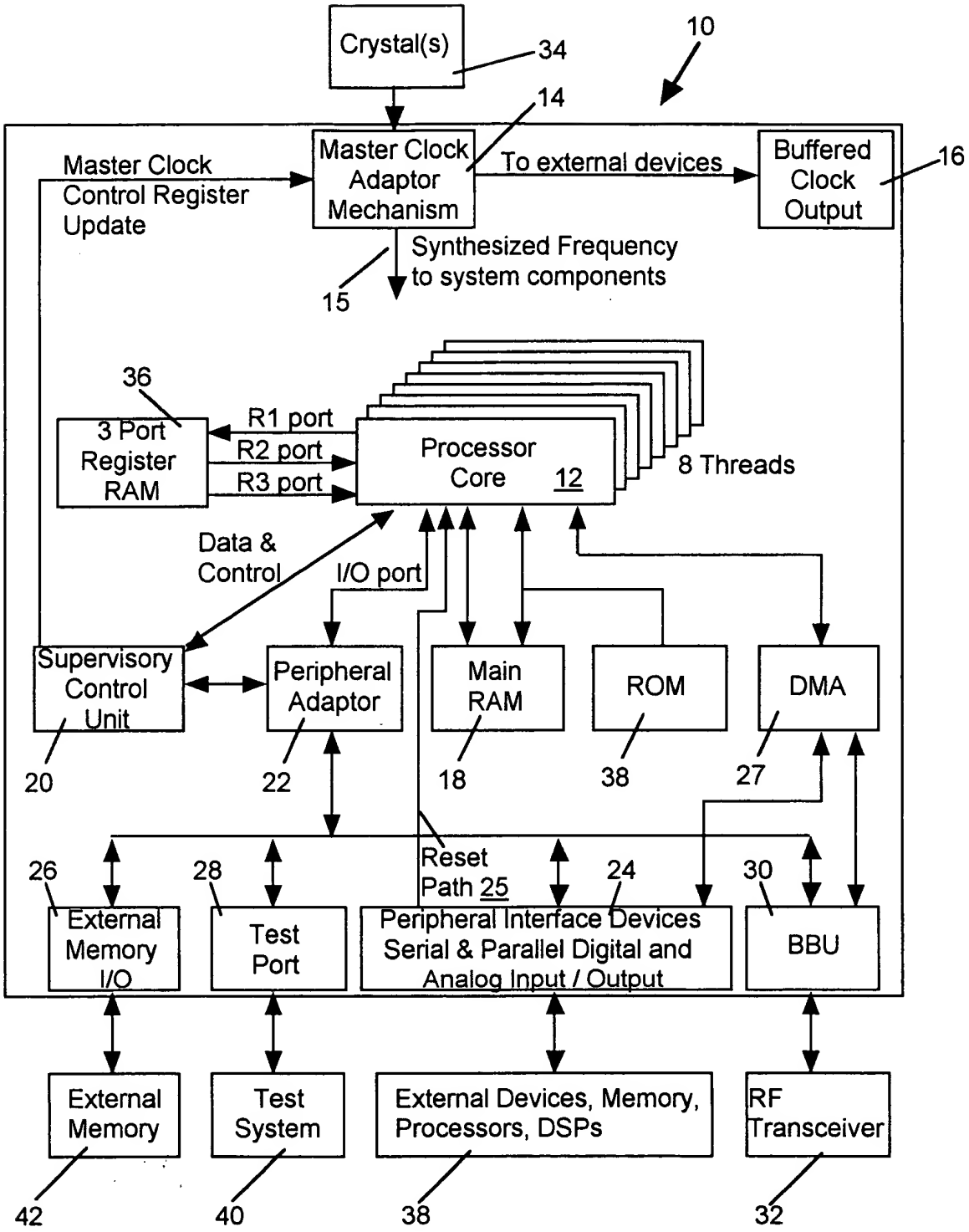

Crystal(s)
34
10
14
Master Clock Adaptor Mechanism
To external devices
Buffered Clock Output
16
Master Clock Control Register Update
Synthesized Frequency to system components
15
36
3 Port Register RAM
R1 port
R2 port
R3 port
Processor Core 12
8 Threads
Data & Control
I/O port
Supervisory Control Unit
Peripheral Adaptor
Main RAM
ROM
DMA
20
22
18
38
27
Reset Path 25
26
28
24
30
External Memory I/O
Test Port
Peripheral Interface Devices Serial & Parallel Digital and Analog Input / Output
BBU
External Memory
Test System
External Devices, Memory, Processors, DSPs
RF Transceiver
42
40
38
32

FIG. 2

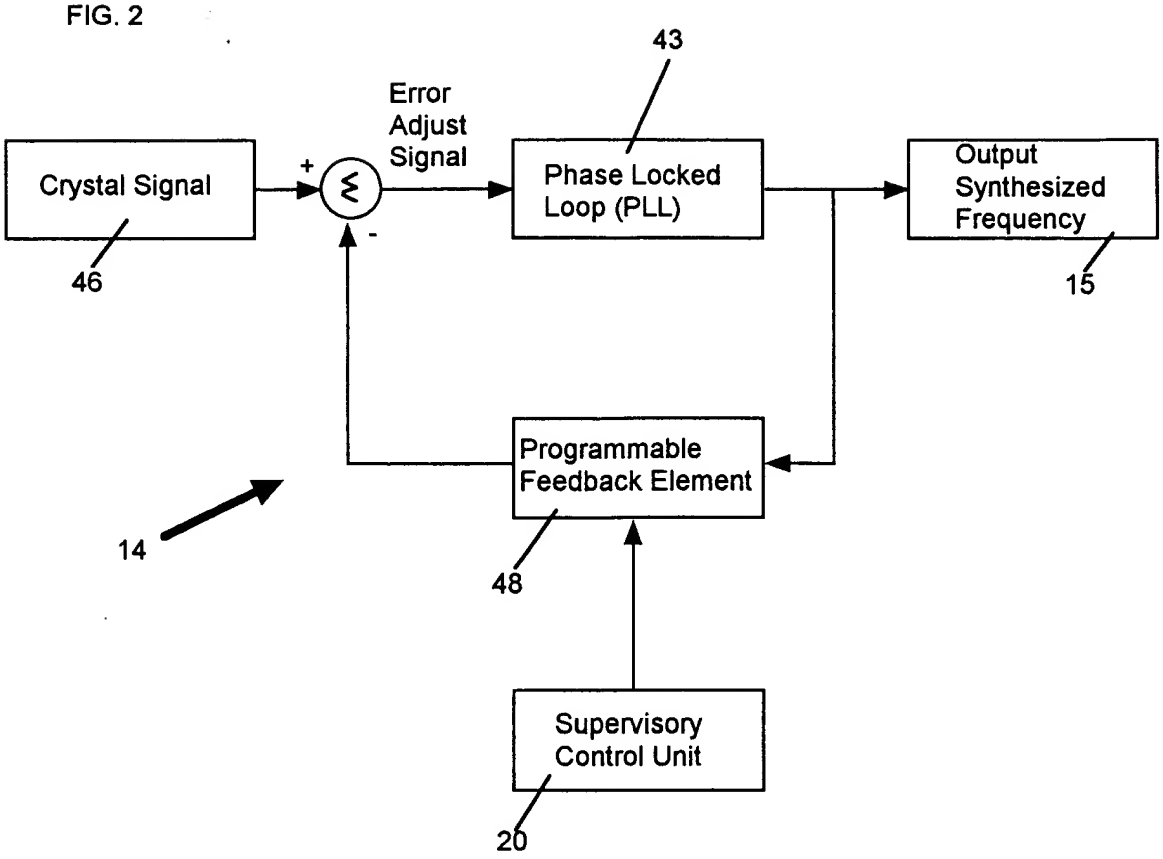


FIG. 3

ADDRESS	READ	WRITE
0	Register R0...R7	Register R0...R7
1	Program Counter	Program Counter
2	Condition Code	Condition Code
3	Break Point	Stop
4	Wait	SCU Access Pointer
5	Semaphore Vector	Up Vector
6	RESERVED	Down Vector
7	Time	Master Clock Control Register

118 120 122 124 126 128 — 130 — 138 136 134 132 112 109 110 44

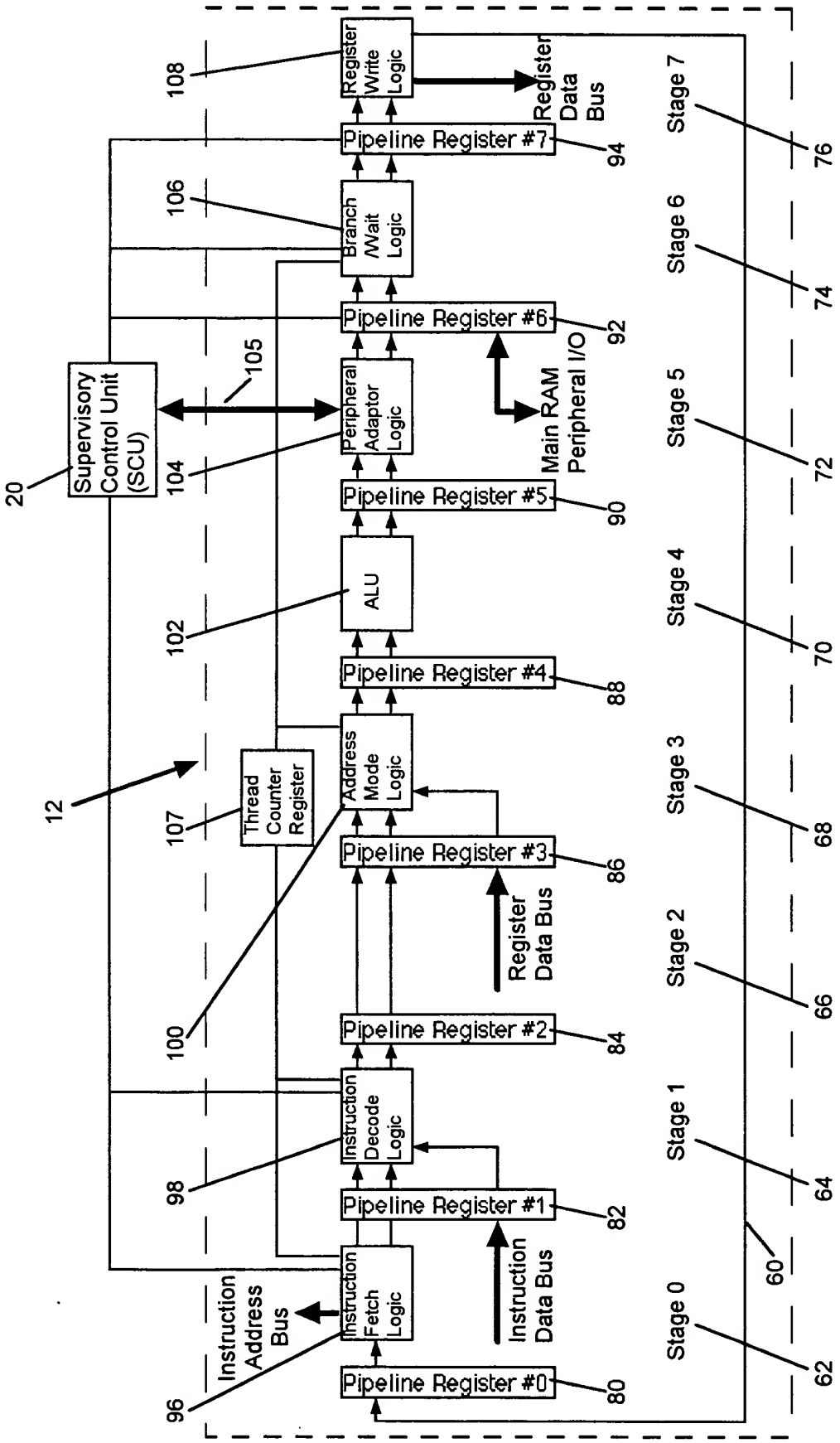

Register Write Logic
Register Data Bus
Pipeline Register #7
Branch /Wait Logic
Pipeline Register #6
Peripheral Adaptor Logic
Main RAM Peripheral I/O
Supervisory Control Unit (SCU)
Pipeline Register #5
ALU
Pipeline Register #4
Address Mode Logic
Thread Counter Register
Pipeline Register #3
Register Data Bus
Pipeline Register #2
Instruction Decode Logic
Pipeline Register #1
Instruction Data Bus
Instruction Fetch Logic
Instruction Address Bus
Pipeline Register #0
Stage 7
Stage 6
Stage 5
Stage 4
Stage 3
Stage 2
Stage 1
Stage 0
108
106
105
104
20
102
107
12
100
98
96
94
92
90
88
86
84
82
80
76
74
72
70
68
66
64
62
60

FIG. 4

FIG. 5

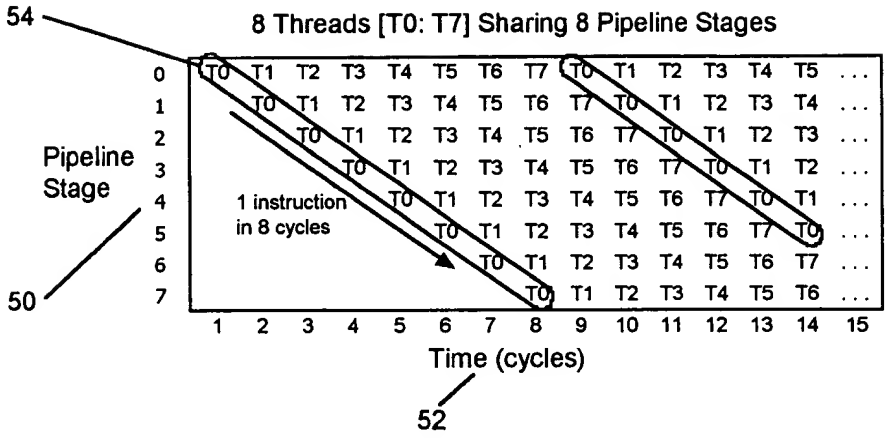


FIG. 6

PIPELINE STAGE Stage #	Description	RESOURCE SAGE - Pr cessor Logic or System Memory: Instruction Fetch Logic	ROM or 2 Port Main RAM	Instruction Decode Logic	Register RAM (3 port)	Address Mode Logic	ALU	Peripheral Adaptor Logic	Branch /Wait Logic	Register Write Logic
0	Instruction Fetch	Used	Read							
1	Instruction Decode			Used						
2	Register Reads				Read					
3	Address Modes					Used				
4	ALU Operation						Used			
5	Memory or I/O Cycle		Read or Write					Read or Write		
6	Branch/Wait								Used	
7	Register Write				Write					Used

58 56

FIG. 7

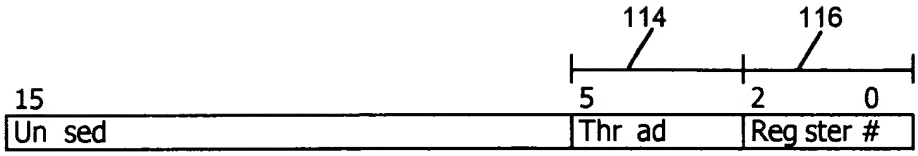
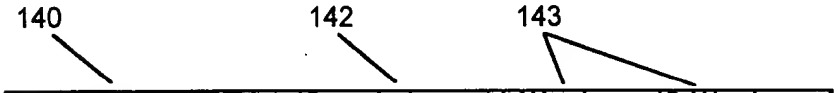


FIG.8

Instr.	Description	Available Address Modes
add	2's complement add	register, immediate
and	bitwise and	register, immediate
bc	conditional branch	PC relative
bic	bit clear	immediate
bis	bit set	immediate
bix	bit change	immediate
bra	unconditional branch	PC relative
inp	read input port	immediate
ior	bitwise inclusive or	register, immediate
jsr	jump to subroutine	register indirect, absolute
ld	load from RAM	base displacement, absolut
mov	move immediate	immediate
outp	write output port	immediate
rol	bitwise rotate left	register, immediate
st	store to RAM	base displacement, absolut
sub	2's complement subtract	register
thrd	get thread number	register
xor	bitwise exclusive or	register, immediate

FIG. 9



Address Mode	Description	1-Word	2-Word
register	Rn	yes	no
register indirect	*Rn	yes	no
base displacement	*(Rn+K)	yes	yes
PC relative	*(PC+K)	yes	yes
absolute	*K	no	yes
immediate	K	some	some